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Research Article

Advanced testing and validation frameworks for high-reliability multi-board electronic systems

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Abstract:

Multi-board digital systems with high reliability are being used in more safety-critical and mission-critical systems, with the failure of such systems potentially having disastrous effects. The conventional rule based and late-stage testing methods cannot handle the increasing system complexity, environmental challenges, and security threats. The paper is a secondary research study of better-level testing and validation structures including intelligent PCB design verification, X-in-the-loop and digital twin-based system validation, fault injection and fuzzing, and non-ideal condition reliability check. The paper summarises the recent research in several areas and reveals the strong points, shortcomings and gaps in integration in the current practice. The results identify the necessity of cross-lifecycle-wide validation frameworks of complex multi-board electronic systems in order to improve key areas of reliability, safety, and resilience.

1. Introduction

The multi-board electronic systems complex systems, including power and electronics, embedded software, sensors and communication interfaces, are becoming more vital in safety-critical and mission-critical applications. Automation of the automotive sector (electrification), aerospace avionics, power grid protection, and industrial automation are in need of constant availability, fault tolerance, and expected performance under less-than-ideal conditions. Increasing functional density, miniaturisation, and inter-board interdependence has led to further significant demands on the need to assure system-level reliability and safety. The traditional methods of testing are still rule-based, manual, and focused at the end of the development, thus restricting their capacity to identify non-linear interactions, transient defects, effects of the environment, and security errors. This paper represents the secondary analysis of testing and validation systems in the advanced to synthesise efficient methods, detect constraints and future research directions in the high-reliability multi-board electronic systems.

2. Research Methodology

2.1 Data Collection and Study Selection

A secondary research methodology is selected in this study to examine and synthesise the existing peer-reviewed literature and authoritative technical reports on advanced testing and validation of high-reliability electronic systems in a scientifically sound manner. The selected articles were identified on the basis of direct relation to safety-critical and mission-critical applications, PCB-level intelligence, multi-board architecture, embedded software validation, power electronic reliability, and system-level reliability. More attention was paid to more recent works that suggest new testing methodologies, fault injection techniques, or lifecycle-based validation approaches.

2.2 Analytical Approach and Synthesis Method

In this study, an analytical synthesis methodology is being used. The identified studies have been reviewed qualitatively to find out the conclusion validation paradigms, the methodological innovations, and the performance outcomes. Each work is classified as per its main area of validation, such as design time verification, system level test, fault injection and integrity checking, environmental resilience and functional safety

expression. The strengths, limitations and complementarities within each of these categories are then compared, which makes possible the derivation of cross-domain insights applicable to high-reliability multi-board electronic systems.

3. Results

3.1 Advanced Design-Time Testing and Intelligent PCB Validation

AI-Driven PCB Design Verification

According to the recent developments in PCB design validation, it is evident that the old rule-based, expert-driven design process has been replaced by data-driven and intelligence-based design processes. Kumar and Veerandra (2020) suggest an end-to-end smart PCB design and in-line testing pipeline approach that explicitly works around the shortcomings of traditional design verification, specifically, their reliance on non-registry scaling in multiple aspects, especially their inability to cope with the non-linear nature of many layout dependencies. They incorporate artificial intelligence even at the design phase, thus allowing verification against design instead of one after design.

Hybrid MLP–GRU Architecture for Defect Diagnosis

The most significant value of the suggested framework is its hybrid Multi-Layer Perceptron and Gated Recurrent Unit architecture. The PCB layouts have high-dimensional spatial features converted to MLP component that represent complicated geometric and connectivity patterns. Simultaneously, the GRU converts serial electrical test signals, which allows real time problem detection and classification. This hybridisation enables the simultaneous space and time analysis and enhances generalisation and flexibility over independent models (Kumar and Veerandra, 2020).

Integrated Optimisation and Validation Outcomes

XGBoost is used to accelerate design rule checking and simulated annealing layout optimisation is used to establish a close collaborative design validation cycle. The experimental outcome has indicated a 31.2 percent decrease in time of design validation and enhanced wrongdoer finding correctness with routing capability equilibrium stabilised following cyclic optimisation. These results have shown that a significant decrease in the necessity to use manual intervention has taken place and there is a high possibility of early fault detection in multi-board electronic assemblies with complex designs where the error committed at design phase is passed onto other boards.

3.2 System-Level Testing Using X-in-the-Loop and Digital Twin Frameworks

Transition from Component-Level to System-Level Validation

With the move towards tightly coupled multi-board architectures with electronic systems, validation has increasingly become less about tests of individual components and more about system-level tests. Leighton et al. (2021) further point out that electrical subsystem testing, such as in power electronics and control units need to be done at a relatively early stage, to bring complexity under control, minimize rework, and enhance the maturity of the entire system. The performance, efficiency and reliability evaluation can be done prior to full physical integration through this philosophy of bottom-up validation.

X-in-the-Loop Testing and Real-Time Fault Injection

The modern system-level validation nowadays is built upon hardware-in-the-loop and software-in-the-loop. Abboush et al. (2024), virtual testing framework, which combines both HIL simulation and programmatic real-time fault injection, is introduced to check the system behaviour in abnormal conditions. Compared to traditional techniques, faults are added without changing system architecture, and real-time constraints are not violated and allow faults of both single and simultaneous sensors and actuators to be analyzed. The measured average relative error of 2.52 is a high fidelity as compared to non-real-time simulations.

Digital Twin–Enabled Continuous Validation

Digital twin integration also builds on XIL by allowing the establishment of a continuous feedback between virtual and real model systems. As a framework, Software-in-the-Loop and Hardware-in-the-Loop testing match with development milestones across the V-cycle, as suggested by Balan et al. (2025). It facilitates refinement and early fault detection, less reliance on physical prototyping and lifecycle-wide validation and is especially useful in regard to high-reliability multi-board electronic systems where there are strict safety and cost requirements.

3.3 Fault Injection, Fuzzing, and Multi-Board Integrity Verification

Golden-Free Detection Strategies for Multi-Board Systems

The integrity of multi-board electronic systems of complexity is becoming more difficult to ensure because of the proliferation of commercial-off-the-shelf parts and supply chains spanning the whole world. Karri et al. (2021) offers a solution to such an issue by introducing a golden-free system of detection that does not use any form of a known-good reference system. Rather than making the assumption that one is familiar with malicious Implant or fault behaviour, the method represents a graph of a networked PCB system and implements the properties of equivalence and invariance across interconnects and nodes. This allows detection of anomalies on a board level and system level without relying on hardware that is trusted.

Multi-Modal Side-Channel Monitoring and Data Fusion

The proposed framework uses multi-modal side-channel data such as hardware performance counters, processor utilisation, temperature, and power consumption in order to track system behaviour during the runtime. The combination of these mixed signals allows one to visualize slight variations due to hardware Trojans, manipulation of firmware or inter board interference. The anomaly detectors based on machine learning are trained on simulator-based proxy data, which enhances scalability and removes the need to utilize physical device data during training (Karri et al., 2021).

Controlled Excitation and Anomaly Amplification

Hardware and software-level fuzzing is used in order to opportunistically anger dormant faults and malicious implants into becoming more visible in side-channel signals. The strategic awareness of excitation improves sensitivity of detection putting strain on alternative lines of communication among boards and implementation streams. It is a unified approach that offers a strong integrity checking approach to COTS based multi-board systems, which tackles reliability and security issues with a non-disruptive approach to normal system operation.

3.4 Reliability and Safety-Oriented Validation Under Non-Ideal Conditions

Radiation-Induced Faults and Environmental Stress Validation

The use of high-reliability electronic systems in power systems, aerospace, and other important infrastructure is subjected to less-than-ideal environmental conditions that may cause latent and transient faults. Zhou et al. (2025) provide a system-level reliability evaluation of relay protection devices that are exposed to the single event effects of radiation. They combine a-particle radiation testing, fault injection with Monte Carlo simulation to calculate the soft error probabilities of realistic workloads. This multi-method validation plan illustrates how environmental stressors may be both systematically analyzed at processor and system levels, with low cost and yet effective information obtained about reliability risks with continuously running electronic systems.

EMC-Aware Virtual Validation at Design Stage

Another important non-ideal case that is a concern of system reliability is electromagnetic compatibility, especially in multi-board, densely-integrated architecture. Amblard et al. (2025) suggest a virtual EMC qualification model based on IBIS modelling to model conducted susceptibility as well as electromagnetic interaction in airplane equipment. This can be used to identify EMC vulnerabilities early in the design phase, preventing expensive late-stage redesign to fix it and making the design more robust prior to physical prototyping by enabling testing of virtual bulk current injection during the design phase.

Functional Safety and Emergency Operation Considerations

The financial safety necessities require predictable behaviour when the fault occurs. According to Kilian et al. (2022), emergency operation strategies are examined in the framework of ISO 26262-conformant power supply systems, thus it is necessary to consider both random hardware occurrences and systematic influences. They highlight that time-constrained emergency operations tracking and fault accumulation as critical validation aspects to secure safe operation continuity cannot be ensured during full functionality loss.

4. Discussion

The literature reviewed shows that there has been a gradual transition away of single verification activities to multi-layered verification paradigms that apply to the increasingly complex high-reliability digital systems that are multi-board. During the design phase, AI-based PCB validation tools show significant efficiency improvement in defect detection rates and less validation time, scalability is assisted in dense electronic design, and with large electronics layouts (Kumar and Veerandra, 2020). Nevertheless, they are still largely limited to board-level artefacts and do not thoroughly answer emergent system-level behaviours as a result of board interconnections and software hardware connecting (Szczesniak et al.,

2021).X-in-the-loop and digital twin System-level checks offer increased coverage and can perform real-time fault injection, tests of virtual scenarios and lifecycle feedback (Abboush et al., 2024; Balan et al., 2025). Although these approaches are useful in increasing validation level and lowering physical prototyping expenses, modelling fidelity and integration cost burden limits their applicability, as pointed out in advanced drive-line and embedded system testing scenarios (Leighton et al., 2021). Fuzzy- and multi-modal side-channel techniques that build on security- and integrity-focused methods provide high protection against hidden faults and malicious implants in multi-board systems based on COTS but raise the problem of training data representativeness and cross-domain generalisation (Karri et al., 2021).The concept of reliability validation in the non-ideal conditions of radiation exposure, electromagnetic influence, and emergency operation cases implies critical operational threats that are commonly ignored in the traditional working process (Zhou et al., 2025; Amblard et al., 2025; Kilian et al., 2022). However, such procedures are normally specific to domains. The major shortcoming in the literature is that no one, lifecycle-supersizing validation framework incorporating intelligent design-time verification and system-level testing verification, fault injection, environmental resilience, and functional safety correspondence, is yet in existence, cutting across domains (Liao, 2024; Okoh and Myklebust, 2024).

5. Conclusions

This secondary study was the review of superior testing and verification systems of high-reliability multi-board electronic systems that run safety and mission-critical application areas. As it was discovered, intelligence-based design-time verification, system level X-in-the-loop testing, fault injection, and environmental stress validation offer solutions to unique problems to reliability. Such methods are also used individually and are specific to domains, though. The results have shown serious issues concerning the unified and life cycle-oriented validation architectures which need to combine the design intelligence, real-time system validation, security assurance, and functional safety compliance. The development of such attempted structures is needed to provide reliable functioning, minimization of latent failure aspects, and to meet the increasing complexity of the modern multi-board electronic systems.

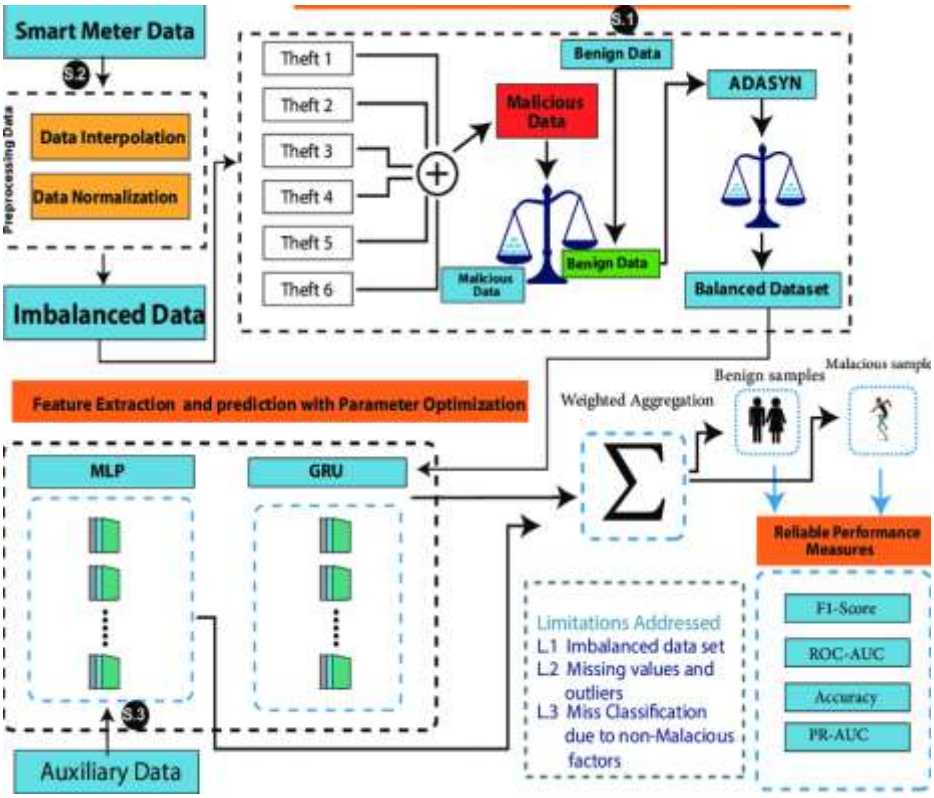

Figure 1: *MLP-GRU model architecture (Kabir et al., 2021)*

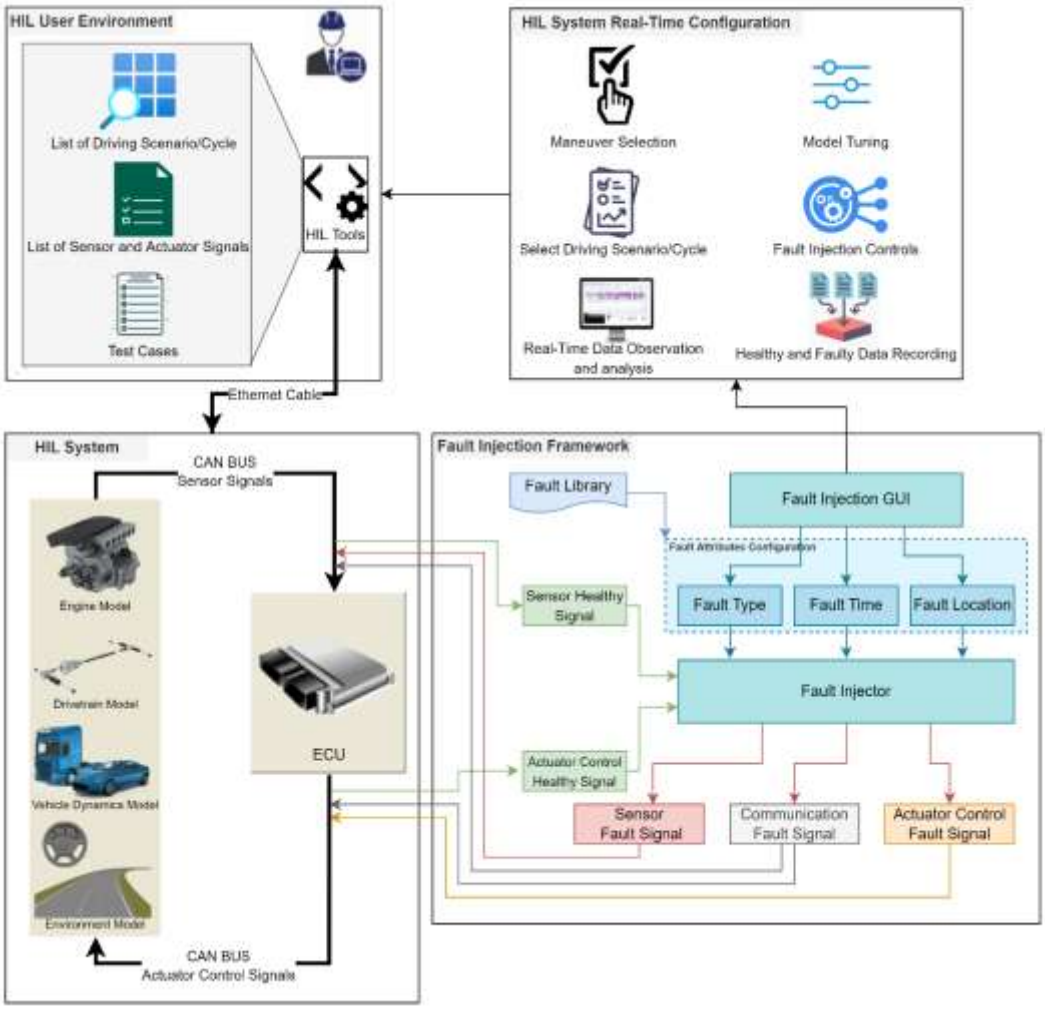

Figure 2: *HiL-based real-time fault injection framework (Kabir et al., 2021)*

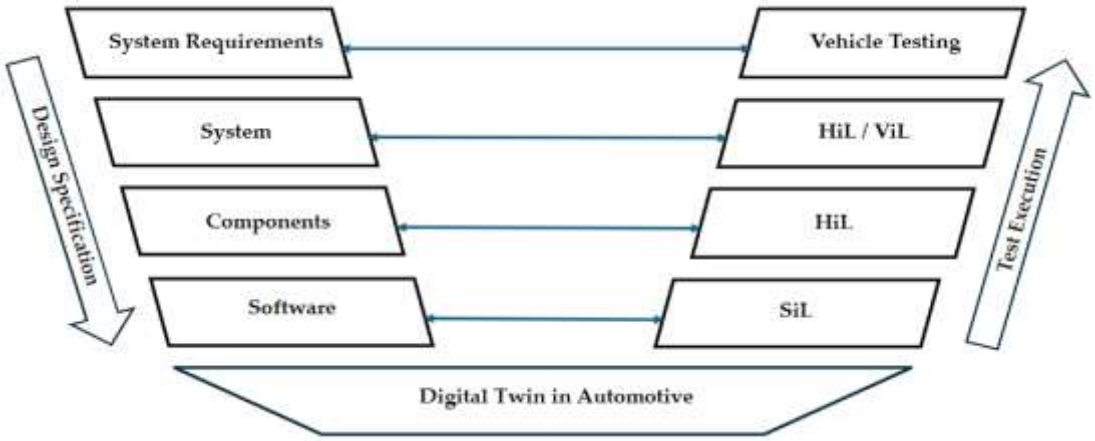

Figure 3: *V-Cycle development process (Balan et al., 2025)*

Author Statements:

- **Ethical approval:** The conducted research is not related to either human or animal use.
- **Conflict of interest:** The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper
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on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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